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Ryo KUBOTO, et al.

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For: MANUFACTURING METHOD OF SEMICONDUCTOR DEVICE HAVING DRAM CAPACITORS

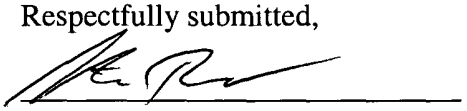
SUBMISSION OF VERIFIED ENGLISH-LANGUAGE TRANSLATION OF PRIORITY DOCUMENT

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Submitted herewith is a verified English-language translation of the priority document on which a claim to priority was made under 35 U.S.C. § 119. The Examiner is respectfully requested to acknowledge receipt of said translation.

Respectfully submitted,



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Enclosure: **Verified English-language translation of Japanese Patent App. No. 094325/2000**

Date: July 11, 2003

DECLARATION

I, the undersigned, Shoji EGUCHI, c/o NEC Electronics Corporation, of 1753 Shimonumabe, Nakahara-ku, Kawasaki, Kanagawa 211-8668, Japan, do hereby solemnly and sincerely declare that I am familiar with the English and Japanese languages, that I have prepared the attached English translation which is a full, true and faithful one of the patent application filed with the Patent Office of Japan under the Application No. 094325/2000 and that the present declaration is intended for use in connection with a patent application placed before the United States Patent and Trademark Office.

I further declare that all statements made herein in my own knowledge and belief are true and that all statements made on information and belief are believed to be true, and further that these statements were made with the knowledge that wilful false statements and the like so made are punishable by fine or imprisonment or both, under Section 1001 of Title 18 of the United States Code and that such wilful false statements may jeopardize the validity of the application or any patent issuing thereon.

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[Title of the Invention]

Method of Manufacturing Semiconductor Device

[Scope of Claim]

[Claim 1] A method of manufacturing a system-on-chip semiconductor device having a CMOS logic circuit portion and a DRAM portion mixedly mounted thereon, said DRAM portion having a cylinder type capacitor lower electrode formed of polysilicon, comprising:

a first step of forming transistors of said CMOS logic circuit portion and of said DRAM portion, respectively;

a second step of forming an interlayer film over the whole surface and forming a groove portion in said interlayer film;

a third step of forming a polysilicon film over the whole surface and forming HSG on the surface of said polysilicon film; and

a fourth step of removing said polysilicon film except in said groove portion to form said capacitor lower electrode.

[Claim 2] A method of manufacturing a semiconductor device as claimed in claim 1, wherein said interlayer film includes BPSG.

[Claim 3] A method of manufacturing a semiconductor device as claimed in claim 1 or 2, wherein boron is implanted in a gate electrode formed of polysilicon of a p-channel transistor of said CMOS logic portion.

[Detailed Description of the Invention]

[0001]

[Technical Filed to which the Invention belongs]

The present invention relates to a method of manufacturing a semiconductor device having a CMOS logic circuit portion and a DRAM mixedly mounted on one chip.

[0002]

[Prior Art]

In a general-purpose DRAM, a plurality of memory cells for storing information and peripheral circuits formed of a decoding circuit and the like for selecting a memory cell are formed on the same semiconductor substrate.

[0003]

A memory cell is provided with a capacitor element for storing information by accumulating signal charge, and a transistor as a switching element for accumulating signal charge in the capacitor element and for reading signal charge accumulated in the capacitor element. It is to be noted that, as the transistor, an FET (Field Effect Transistor) of MOS (Metal Oxide Semiconductor) structure or of MIS (Metal Insulator Semiconductor) structure is used since they are advantageous in making the integration higher. As a transistor for the peripheral circuit, an FET having the same structure as that of the memory cell is used for the purpose of unifying its manufacturing process

to that of the memory cell.

[0004]

In these days, memory cells of general-purpose DRAMs are required to be miniaturized more and more for the purpose of making higher the integration of the general-purpose DRAM. However, since the capacitance value of a capacitor element basically depends on the area of electrodes and the relative dielectric constant of an insulating film sandwiched therebetween, special measures are required to be taken to accomplish both large capacitance and miniaturization. Therefore, to form a capacitor element in a three-dimensional structure has been considered to secure desired capacitance. For example, a cylinder structure shown in Fig. 4 and a stack structure shown in Fig. 5 have been adopted.

[0005]

Fig. 4 is a sectional side elevation showing the structure of a part of a general-purpose DRAM having capacitor elements of the cylinder structure, and Fig. 5 is a sectional side elevation showing the structure of a part of a general-purpose DRAM having capacitor elements of the stack structure.

[0006]

As shown in Fig. 4, in the capacitor element of the cylinder structure, a groove (Cylinder 103) is formed in an interlayer film 102 formed on the whole surface of a substrate. A lower electrode

(hereinafter also referred to as a capacitor lower electrode) 104 formed of a polysilicon film with impurity such as phosphorus (P) implanted therein, a capacitor film 105 formed of an Si_3N_4 film, a Ta_2O_5 film, or the like, and an upper electrode 107 formed of a polysilicon film similar to that of the lower electrode 104 are structured to be laminated in this order along the inner wall of the cylinder 103. By forming the cylinder 103 deeply, the surface area of the lower electrode 104 and of the upper electrode 107 is made large.

[0007]

It is to be noted that, in a case a polysilicon film is used and the lower electrode 104 of the capacitor element, a method where minute unevenness is provided on the surface of the lower electrode 104 to make the surface area large has been attempted. More specifically, spherical or hemispherical grains called HSG (Hemispherical Grained Polysilicon) are formed on the surface of the lower electrode 104. In a case a Ta_2O_5 film is used as the capacitor film 105, a titanium nitride (TiN) film 106 is formed on the Ta_2O_5 film for suppressing the reaction between the Ta_2O_5 film and polysilicon.

[0008]

On the other hand, as shown in Fig. 5, in the capacitor element of the stack structure, a convex-shaped lower electrode 204 formed of a polysilicon film with impurity such as phosphorus

(P) implanted therein is formed on an interlayer insulating film 202 formed on the whole surface of a substrate. A capacitor film 205 formed of an Si_3N_4 film, a Ta_2O_5 film, or the like, and an upper electrode 207 formed of a polysilicon film similar to that of the lower electrode 204 are structured to be laminated in this order on the lower electrode 204. By forming the convex-shaped lower electrode 204 so as to be large, the surface area of the lower electrode 204 and of the upper electrode 207 are made large. It is to be noted that, in a case a polysilicon film is used as the lower electrode 204 of the capacitor element, as shown in Fig. 5, HSG 206 is formed to make large the surface area of the lower electrode 204.

[0009]

Next, a method of manufacturing a semiconductor device (general-purpose DRAM) having the above capacitor element is described using Figs. 6-9.

[0010]

Figs. 6 and 7 are sectional side elevations showing a fabrication process of a semiconductor device having the capacitor element of the conventional cylinder structure. Fig. 8 is a sectional side elevation showing another fabrication process of a semiconductor device having the capacitor element of the conventional cylinder structure. Fig. 9 is a sectional side elevation showing a fabrication process of a semiconductor

device having the capacitor element of the conventional stack structure.

[0011]

It is to be noted that, with Figs. 6-9, a case where, as transistors for memory cells, n-channel transistors having the MOS structure are formed on a p-type semiconductor substrate is described. It is also to be noted that, though transistors for the peripheral circuits are not shown in Figs. 6-9, the structure of n-channel transistors for the peripheral circuits is the same as that of the transistors for the memory cells, and the structure of p-channel transistors is basically the same except that the kind of impurity in a channel region and in a source / drain region is different.

[0012]

First, examples of the method of manufacturing the general-purpose DRAM having the capacitor element of the cylinder structure are described using Figs. 6-8.

[0013]

First, as element separating regions 111 for separating the respective transistors, grooves (STI: shallow Trench Isolation) having uniform depth and filled with an oxide film is formed on a p-type semiconductor substrate 110 using a conventional method (Fig. 6(a)).

[0014]

Then, after boron (B), for example, is implanted in a region for forming a transistor to form a channel region (not shown), a gate oxide film 112 at the thickness of about 70 -80 angstrom is formed by thermal oxidation of the surface of the p-type semiconductor substrate 110. Further, a polysillicon film at the thickness of about 1500 angstrom (3000 angstrom or less) to be a gate electrode is formed on the gate oxide film 112 by CVD. By patterning them in a desired shape using photolithography, a gate electrode 113 is formed.

[0015]

Then, arsenic (As) or phosphorus is implanted in the p-type semiconductor substrate 110 with the gate electrode 113 being used as a mask to form an SD extension region (not shown). Next, an insulating film which is a silicon oxide film, silicon nitride film, or multilayer of them is deposited over the whole surface and etching back is carried out to form side walls 114 on side surfaces of the gate electrode 113. Then, with the gate electrode 113 and the side walls 114 being used as the mask, arsenic or phosphorus is implanted in the p-type semiconductor substrate 110 to form a source / drain region 115 (Fig. 6(b)).

[0016]

Then, an interlayer insulating film 116 formed of SiO_2 at the thickness of 5000 -8000 angstrom is formed over the whole surface using atmospheric pressure CVD. A photoresist 117 is

formed on the interlayer insulating film 116, patterning is carried out, and the interlayer insulating film 116 in an opening of the photoresist 117 is etched and removed, and a capacitor contact 118 formed which connects a drain of the transistor to the upper surface of the interlayer insulating film 116 (Fig. 6(c)). It is to be noted that the interlayer insulating film 116 may be structured to include BPSG (Borophosphosilicate Glass).

[0017]

Then, after the photoresist 117 is removed, a capacitor electrode 119 formed of a phosphorus doped polysilicon film, for example, is buried the capacitor contact 118. Further, a cylinder interlayer film 120 formed of BPSG or the like at the thickness of 6000 - 14000 angstrom is formed on the interlayer insulating film 116, and heat treatment is carried out at about 800℃ - 850℃ for about 10 - 30 minutes to bake BPSG. It is to be noted that the cylinder interlayer film 120 may be structured such that an SiO_2 film deposited by atmospheric pressure CVD on the BPSG film.

[0018]

Next, a photoresist 121 is coated on the whole surface, patterning is carried out, the cylinder interlayer film 120 in an opening of the photoresist 121 is etched and removed, and a groove (cylinder 122) which connects the capacitor contact 118 and the upper surface of the cylinder interlayer film 120 is formed (Fig. 6(d)). A capacitor element for the DRAM is formed in the

cylinder 122 formed here.

[0019]

Then, after photoresist 121 is removed, a polysilicon film to be a lower electrode 123 of the capacitor element with phosphorus doped therein (dose: about 1×10^{19} - 1×10^{20} atoms/cm^3) and at the thickness of about 1500 - 3000 angstrom is formed all over the surface including the inner wall of the cylinder 122 (Fig. 7(e)). Further, a photoresist 124 is formed over the whole surface patterning is carried out such that the photoresist 124 is left only in the cylinder 122, and the polysilicon film on the cylinder interlayer film 120 is etched and removed.

[0020]

Next, after the photoresist 124 in the cylinder 122 is removed, annealing (at about 500 - 600℃ for about 10 -60 minutes) is carried out with silane (SiH_4) irradiated thereon to form nuclei of HSG on the lower electrode. Further, by annealing in a vacuum (at 500 - 600℃ for 10 - 60 minutes), grains are made to grow around the nuclei to form HSG 124 (Fig. 7(f)).

[0021]

Finally, a capacitor film 126, a TiN film 127, and an upper electrode 128 formed of polysilicon with phosphorus doped therein are formed in this order on the layer electrode 123 (Fig. 7(g)). Wiring follows using a conventional process.

[0022]

It is to be noted that, though Fig. 7(g) shows that HSG 125 on the lower electrode 123 is omitted for the sake of simplicity of the drawing, actually, as shown in Fig. 7(f), the HSG 125 is formed on the lower electrode 123.

[0023]

Further, though, in the above process, the HSG 125 is made to grow in the cylinder 122 after the polysilicon film on the cylinder interlayer film 120 is removed by etching back, it may be that, as shown in Fig. 8, after the HSG 125 is formed on the polysilicon film on the cylinder interlayer film 120 and in the cylinder 122, the polysilicon film and the HSG 125 on the cylinder interlayer film 120 are removed by etching back to leave the polysilicon film (lower electrode 123) and the HSG 125 in the cylinder 122. Such a procedure is disclosed in, for example, Japanese Patent Application Laid-open No. Hei 11-284139.

[0024]

Next, an example of the method of manufacturing the general-purpose DRAM having the capacitor element of the stack structure is described using Fig. 9.

[0025]

First, as shown in Figs. 6(a) - (c), similarly to the fabrication process of the general-purpose DRAM having the capacitor element of the cylinder structure, an element separating regions 211 and a transistor are formed on a p-type

semiconductor substrate 210. After an interlayer insulating film 216 is formed over the whole surface, a capacitor contact 218 is formed. It is to be noted that interlayer insulating film 216 is structured to be a BPSG film with an SiO_2 film deposited thereto which is formed using atmospheric pressure CVD.

[0026]

Then, a capacitor electrode 219 formed of a polysilicon film with phosphorus doped therein is buried in the capacitor contact 218 (Fig. 9(a)), and a phosphorus doped polysilicon film (dose: about $1 \times 10^{19} - 1 \times 10^{20}$ atoms/cm^3) and at the thickness of about 6000 - 10000 angstrom is formed all over the surface. Then, a photoresist 224 is formed over the whole surface, patterning is carried out such that the photoresist 224 is left only in a region to be a lower electrode 223 of the capacitor element (Fig. 9(b)), and the unnecessary polysilicon film 222 on the interlayer insulating film 216 is etched and removed to form the lower electrode 223.

[0027]

Next, after the photoresist 224 is removed, annealing (at about 500 - 600℃ for about 10 - 60 minutes) is carried out with silane (SiH_4) irradiated thereon to form nuclei of HSG on the lower electrode 223. Further, by annealing in a vacuum (at 500 - 600℃ for 10 - 60 minutes), grains are made to grow around the nuclei to form HSG 224 (Fig. 9(c)).

[0028]

Finally, a capacitor film 227 and a upper electrode 228 formed of phosphorus doped polysilicon are formed in this order on the lower electrode 223 (Fig. 9(d)). Wiring follows using a conventional process.

[0029]

[Problem to be solved by the Invention]

These days, a semiconductor device not only has a single function of a CPU, a logic circuit, a memory device, or the like, but also has them on one chip to materialize a desired system, which is called as system-on-chip (SOC).

[0030]

In such a semiconductor device having a CMOS logic circuit portion such as a CPU and a logic circuit and a DRAM portion mixedly mounted thereon, when transistors for the CMOS logic circuit portion and transistors for memory cells of the DRAM portion are formed and then capacitor elements of the cylinder structure are formed according to the procedure shown in Figs. 6(c) - 7(g), failure in manufacture arises that the HSG is not normally formed in the growth process of the HSG shown in Fig. 7(f).

[0031]

On the other hand, in a semiconductor device having a CMOS logic circuit portion and a DRAM portion provided with a capacitor element of the stack structure mixedly mounted thereon, when the

capacitor element of the stack structure is formed according to the procedure shown in Fig. 9(a) - (d), the HSG is normally formed in the growth process of the HSG shown in Fig. 9(c).

[0032]

More specifically, the HSG is not normally formed only when, in a structure where a CMOS logic circuit portion and a DRAM portion provided with a capacitor element of the cylinder structure are mixedly mounted, a polysilicon film is formed on a cylinder interlayer film and in a cylinder, the polysilicon film on the cylinder interlayer film is removed by etching back, and then the HSG is formed in the cylinder. This is a problem which arises even when the conditions of formation of the HSG (nucleation time period of the HSG, annealing time period, and the like) are changed, and has repeatability.

[0033]

It is to be noted that, in a capacitor element of the stack structure, the lower electrodes formed in the process shown in Fig. 9(c) are liable to fall down, and, if the distance between the lower electrodes is small, failure in fabrication arises that the HSG's are connected to each other. In particular, when both making it finer and making its capacitance larger are attempted, it is necessary that thin and tall lower electrodes are formed closely, and thus, the above failure fabrication are more liable to arise. Therefore, in a semiconductor device of the next

generation which is required to have higher integration, it is preferable that the cylinder structure rather than the stack structure is used as the capacitor elements.

[0034]

The present invention is made to solve the above problem of the prior art, and an object of the present invention is to provide a method of manufacturing a semiconductor device where HSG can be formed without fail on lower electrodes in cylinders for capacitor elements even when the semiconductor device has a CMOS logic circuit portion and a DRAM portion provided with a capacitor element of the cylinder structure mixedly mounted theron.

[0035]

[Means for solving the Problem]

In order to attain the above object, a method of manufacturing a semiconductor device according to the present invention is a method of manufacturing a system-on-chip semiconductor device having a CMOS logic circuit portion and a DRAM portion mixedly mounted thereon, the DRAM portion having a cylinder type capacitor lower electrode formed of polysilicon, comprising a first step of forming transistors of the CMOS logic circuit portion and of the DRAM portion, respectively, a second step of forming an interlayer film over the whole surface and forming an groove portion in the interlayer film, a third step

of forming a polysilicon film over the whole surface and forming HSG on the surface of the polysilicon film, and a fourth step of removing the polysilicon film except in the groove portion and forming the capacitor lower electrode.

[0036]

Here, the interlayer film includes BPSG, and boron is implanted in a gate electrode formed of polysilicon of a p-channel transistor of the CMOS logic portion.

[0037]

It the above method of manufacturing a semiconductor device, by, after the HSG is formed on the polysilicon film formed on the interlayer film and in the cylinder, removing the polysilicon film and the HSG on the interlayer film with the polysilicon film and the HSG in the cylinder being left, the HSG can be formed without fail in the cylinder even when the semiconductor device has a CMOS logic circuit portion and a DRAM portion mixedly mounted thereon.

[0038]

[Embodiment Mode of the Invention]

Next, the present invention is described with reference to the drawings.

[0039]

A method of manufacturing a semiconductor device according to the present invention is a method where, when a semiconductor device having a CMOS logic circuit portion and a DRAM portion

mixedly mounted thereon is formed, the DRAM portion being provided with a capacitor element of the cylinder structure, similar to the manufacturing process of a general-purpose DRAM shown in Fig. 8, after HSG is formed on a cylinder interlayer film and on a polysilicon film in a cylinder, the polysilicon film and the HSG on the cylinder interlayer film are removed, respectively, with the polysilicon film and the HSG in the cylinder being left.

[0040]

The inventor has found that, by manufacturing according to the above procedure a capacitor element of a semiconductor device having a CMOS logic circuit portion and a DRAM portion provided with the capacitor element of the cylinder structure mixedly mounted thereon, the HSG is formed in the cylinder without fail.

[0041]

The reason for this is not clear, but the cylinder interlayer film exposed by removing the polysilicon film before forming the HSG is thought to influence the abnormal growth of the HSG in the procedure of forming the HSG in the cylinder after the polysilicon film on the cylinder interlayer film is removed.

[0042]

More specifically, in a general-purpose DRAM, as shown in Fig. 1(a), for example, memory cells 1 and peripheral circuits 2 are disposed, and the ratio of the memory cells 1 to the area of the chip is 50 - 60%. On the other hand, in a semiconductor

device with a CMOS logic circuit portion and a DRAM portion mixedly mounted thereon, as shown in Fig. 1(b), for example, since a CMOS logic circuit portion 3, memory cells 1 for the DRAM, and peripheral circuit 2 are dispose, the ratio of the memory cells 1 to the area of the chip is 10 - 25 %. Therefore, in a general-purpose DRAM, the ratio of a cylinder interlayer film exposed when HSG is formed to the area of the chip is small, whereas, in a semiconductor device with a CMOS logic circuit portion and a DRAM portion mixedly mounted thereon, the ratio of a cylinder interlayer film to the area of the chip is large.

[0043]

Further, though, in a general-purpose DRAM, BPSG in a cylinder interlayer film can be baked by carrying out heat treatment at about 800℃ - 850℃ for about 10 - 30 minutes after a cylinder interlayer film is formed, in a semiconductor device with a CMOS logic circuit portion and a DRAM portion mixedly mounted thereon, as described in the following, since the characteristics of transistors for the CMOS logic circuit portion are changed by applying a high temperature (800℃ or above), the above heat treatment can not be carried out. Therefore, unnecessary substances (such as moisture) in the BPSG can not be sufficiently removed, which are thought to adversely affect the growth of HSG.

[0044]

It is to be noted that, though, when a capacitor element of the stack structure is formed, similarly, an interlayer insulating film is exposed when HSG is formed, however it is thought that, since the interlayer insulating film is thinner compared with the cylinder interlayer film, and, in particular, the absolute amount of BPSG is small, the HSG is considered to be normally formed.

[0045]

The reason why heat treatment at a high temperature can not be carried out with regard to a semiconductor device with a CMOS logic circuit portion and a DRAM portion mixedly mounted thereon is as follows.

[0046]

Since high performance such as operating at a high speed is required of a transistor for a CMOS logic circuit portion, boron (B) is implanted in a gate electrode (polysilicon) of a p-channel transistor while phosphorus (P) is implanted in a gate electrode (polysilicon) of an n-channel transistor to make the same kind of impurity in the channels and in the gate electrodes. By this, a depletion area is formed immediately under a gate oxide film to prevent decrease in ON current and decrease in the controllability due to the deep channels. Since, typically, a capacitor element is formed after a transistor is formed, if a high temperature is applied in the process of forming the

capacitor element, boron (B) in the gate electrode of the p-channel transistor of the CMOS logic circuit portion diffuses to reach the inside of the channel through the gate oxide film. By the piercing phenomenon of boron, the threshold voltage Vt of the transistor changes.

[0047]

On the other hand, since high performance is not required of a transistor for a peripheral circuit of a general-purpose DRAM, phosphorus (P) is implanted in a gate electrode (polysilicon) of a p-channel transistor similarly to the case of an n-channel transistor to reduce the number of the processes. Therefore, in such a structure, the above piercing phenomenon of boron does not occur. Further, in case boron is implanted in a gate electrode, since a gate oxide film of a transistor for a peripheral circuit of a general-purpose DRAM is formed to be thicker than that of a transistor for a CMOS logic circuit portion, the above piercing phenomenon of boron does not occur either. It is to be noted that, in a DRAM portion mounted on an SOC semiconductor device, since an existing general-purpose DRAM is mounted at it is as a functional block, generally, the structure of a transistor for a peripheral circuit of a DRAM portion need not be same as that of a transistor for a CMOS logic circuit portion.

[0048]

As described in the above, even with regard to a

semiconductor device with a CMOS logic circuit portion and a DRAM having capacitor elements of the cylinder structure mixedly mounted thereon, by after forming HSG on a polysilicon film on a cylinder interlayer film and in a cylinder, removing the polysilicon film and the HSG on the cylinder interlayer film with the polysilicon film and the HSG in the cylinder being left according to the present invention, the HSG can be formed without fail in the cylinder. Therefore, a capacitor element which has large capacitance and is miniaturized can be formed in a semiconductor device with a CMOS logic circuit portion and DRAM portion mixedly mounted thereon.

[0049]

Next, a method of manufacturing a semiconductor device according to the present invention is described using Figs. 2 and 3. Figs. 2 and 3 are sectional side elevations showing a manufacturing procedure of a semiconductor device according to the present invention. It is to be noted that, with Figs. 2 and 3, a case where a logic portion where a CMOS logic circuit portion is formed has n-channel transistors and p-channel transistors having the MOS structure and memory cells have n-channel transistors of the MOS structure and capacitor elements of the cylinder structure is described. It is also to be noted that the above respective transistors are formed on the same semiconductor substrate. It is also to be noted that, though transistors for

the peripheral circuits of the DRAM portion are not shown in Figs. 2 and 3, the structure of n-channel transistors for the peripheral circuits is the same as that of the transistors for the memory cells, and the structure of p-channel transistors is basically the same except that the kind of impurity in a channel region and in a source / drain region is different.

[0050]

In the method of manufacturing a semiconductor device according to the present invention, as element separating regions 11 for separating the respective transistors for the CMOS logic circuit portion and for the DRAM portion, grooves (STI) having uniform depth and filled with an oxide film is formed on a semiconductor substrate 10 using a conventional method (Fig. 2(a)).

[0051]

Then, boron, for example, is implanted in a p-channel transistor forming region 5 to form an n-well region (not shown) while arsenic or phosphorus is implanted in an n-channel transistor forming region 4 (including a region 6 for forming a transistor for a memory cell) to form a p-well region (not shown). Further, boron is implanted in the n-channel transistor forming regions 4 and 6 to form channel regions (not shown) while arsenic or phosphorus is implanted in the p-channel transistor forming region to form a channel region (not shown).

[0052]

Then, a gate oxide film 112 at the thickness of about 30 - 40 angstrom is formed by thermally oxidizing the surface of the semiconductor substrate 10, and a polysilicon film at the thickness of about 1500 angstrom (3000 angstrom or less) to be a gate electrode is formed on the gate oxide film 12 by CVD. By patterning them in a desired shape using photolithography, gate electrodes 13 of the respective transistors are formed.

[0053]

Then, arsenic or phosphorus is implanted in the n-channel transistor forming regions 4 and 6 with the gate electrode 13 being used as the mask to form an SD extension region (not shown). Similarly, boron is implanted in the p-channel transistor forming region 5 to form an SD extension region (not shown).

[0054]

Next, an insulating film which is a silicon oxide film, silicon nitride film, or multilayer of them is deposited over the whole surface and etching back is carried out to form respective side walls 14 on side surfaces of the respective gate electrodes. Then, with the gate electrode 13 and the side walls 14 being used at the mask, arsenic or phosphorus is implanted in the n-channel transistor forming regions 4 and 6 to form source / drain regions 15 while boron is implanted in the p-channel transistor forming region 5 to form another source / drain region 15 (Fig. 2(b)).

It is to be noted that, depending on the ion implantation process here, arsenic or phosphorus may be implanted in the gate electrodes (polysilicon) of the n-channel transistors and boron may be implanted in the gate electrode of the p-channel transistor.

[0055]

Then, an interlayer insulating film 16 formed of SiO_2 at the thickness of 5000 - 8000 angstrom is formed over the whole surface of the semiconductor substrate 10 using atmospheric pressure CVD. A photoresist 17 is formed on the interlayer insulating film 16, patterning is carried out, and the interlayer insulating film 16 in an opening of the photoresist 17 is etched and removed, and a capacitor contact 18 is formed which connects a drain of the transistor 6 for the memory cell to the upper surface of the interlayer insulating film 16 (Fig. 2(c)). It is to be noted that the interlayer insulating film 16 may be structured to include BPSG.

[0056]

Then, after the photoresist 17 is removed, polysilicon with phosphorus, for example, doped therein is buried by CVD, unnecessary polysilicon is removed by etching back, and a capacitor electrode 19 is formed in the capacitor contact 18.

[0057]

Then, a cylinder interlayer film 20 formed of BPSG at the

thickness of about 6000 - 14000 angstrom is formed over the whole surface. It is to be noted that the cylinder interlayer film 20 may be structured such that an SiO_2 film formed by atmospheric pressure CVD is laminated on the BPSG film.

[0058]

Next, a photoresist 21 is formed on the whole surface, patterning is carried out, the cylinder interlayer film 20 in an opening of the photoresist 21 is etched and removed, and a cylinder 22 as a groove which connects the capacitor contact 18 and the upper surface of the cylinder interlayer film 20 is formed (Fig. 2(d)). A capacitor element for the DRAM is formed in the cylinder 22 formed here.

[0059]

Then, after the photoresist 21 is removed, a phosphorus doped polysilicon (dose: about $1 \times 10^{19} - 1 \times 10^{20}$ atoms/cm^3) film to be a lower electrode 23 of the capacitor element and at the thickness of about 1500 - 3000 angstrom is formed all over the surface including the inner wall of the cylinder 22 (Fig. 3(e)). Next, annealing (at about 500 - 600℃ for about 10 - 60 minutes) is carried out with silane irradiated thereon to form nuclei of HSG on the lower electrode 23 on the cylinder interlayer film 20 and in the cylinder 22. Further, by annealing in a vacuum (at 500 - 600℃ for 10 - 60 minutes), grains are made to grow around the nuclei to form HSG 24 on the polysilicon film on the cylinder

interlayer film 20 and in the cylinder 22.

[0060]

Then, a photoresist 25 is formed over the whole surface, patterning is carried out such that the photoresist 25 is left only in the cylinder 22 (Fig. 3(f)), and the polysilicon film and the HSG 24 on the cylinder interlayer film 20 is etched and removed.

[0061]

Finally, the photoresist 25 in the cylinder 22 is removed, and a capacitor film 26 and an upper electrode 28 formed of polysilicon are formed in this order on the lower electrode 23 (Fig. 3(g)). Wiring follows using a conventional process.

[0062]

It is to be noted that, in a case a Ta_2O_5 film is used as the capacitor film 26, as shown in Fig. 3(g), a TiN film 27 for suppressing the reaction between the Ta_2O_5 film and polysilicon is formed on the Ta_2O_5 film. Further, though Fig. 3(g) shows that the HSG 24 on the lower electrode 23 is omitted for the sake of simplicity of the drawing, actually, as shown in Fig. 3(f), the HSG 24 is formed on the lower electrode 23.

[0063]

[Effects of the Invention]

Since the present invention is structured as described in the above, it has effect as described in the following.

[0064]

By, after HSG is formed on a polysilicon film formed on an interlayer film and in a cylinder, removing the polysilicon film and the HSG on the interlayer film with the polysilicon film and the HSG in the cylinder being left, the HSG can be formed without fail in the cylinder. Therefore, a capacitor element which has high capacitance and is miniaturized can be formed in a semiconductor device with a CMOS logic circuit portion and a DRAM portion mixedly mounted thereon.

[Brief Description of the Drawings]

[Fig. 1] A view showing an example of arrangement of elements of a semiconductor device. Fig 1(a) is a plan view of a general-purpose DRAM, and Fig. 1(b) is a plan view of a semiconductor device with a CMOS logic circuit portion and a DRAM mixedly mounted thereon.

[Fig. 2] A sectional side elevation showing a fabrication process of a semiconductor device according to the present invention.

[Fig. 3] A sectional side elevation showing the fabrication process of a semiconductor device according to the present invention.

[Fig. 4] A sectional side elevation showing the structure of a part of a general-purpose DRAM having capacitor elements of the cylinder structure.

[Fig. 5] A sectional side elevation showing the structure

of a part of a general-purpose DRAM having capacitor elements of the stack structure.

[Fig. 6] A sectional side elevation showing a fabrication process of a semiconductor device having a capacitor element of a conventional cylinder structure.

[Fig. 7] A sectional elevation showing the fabrication process of a semiconductor device having a capacitor element of a conventional cylinder structure.

[Fig. 8] A sectional side elevation showing another fabrication process of a semiconductor device having a capacitor element of a conventional cylinder structure.

[Fig. 9] A sectional side elevation showing a fabrication process of a semiconductor device having a capacitor element of a conventional stack structure.

[Description of Reference Numerals]

1 memory cell

2 peripheral circuit

3 CMOS logic circuit portion

4 n-channel transistor forming region

5 p-channel transistor forming region

6 region for forming transistor for memory cell

10 semiconductor substrate

11 element separating region

12 gate oxide film

13 gate electrode

14 side wall

15 source / drain region

16 interlayer insulating film

17,21,25 photoresist

18 capacitor contact

19 capacitor electrode

20 cylinder interlayer film

22 cylinder

23 lower electrode

24 HSG

26 Ta_2O_5 film

27 TiN film

28 upper electrode

【書類名】　図面
[Name of Document]　Drawings
【図１】　Fig. 1

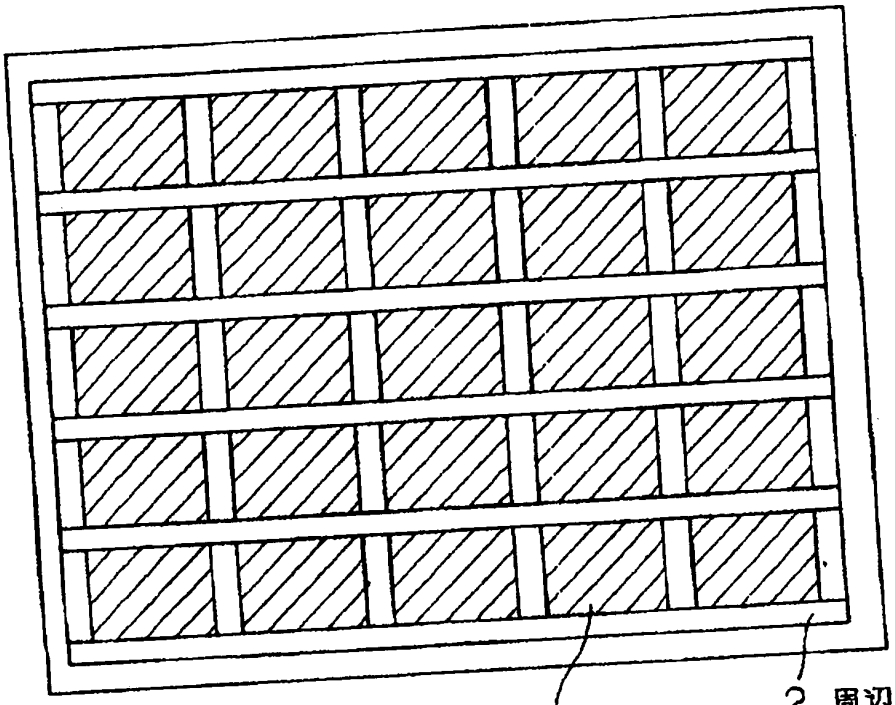
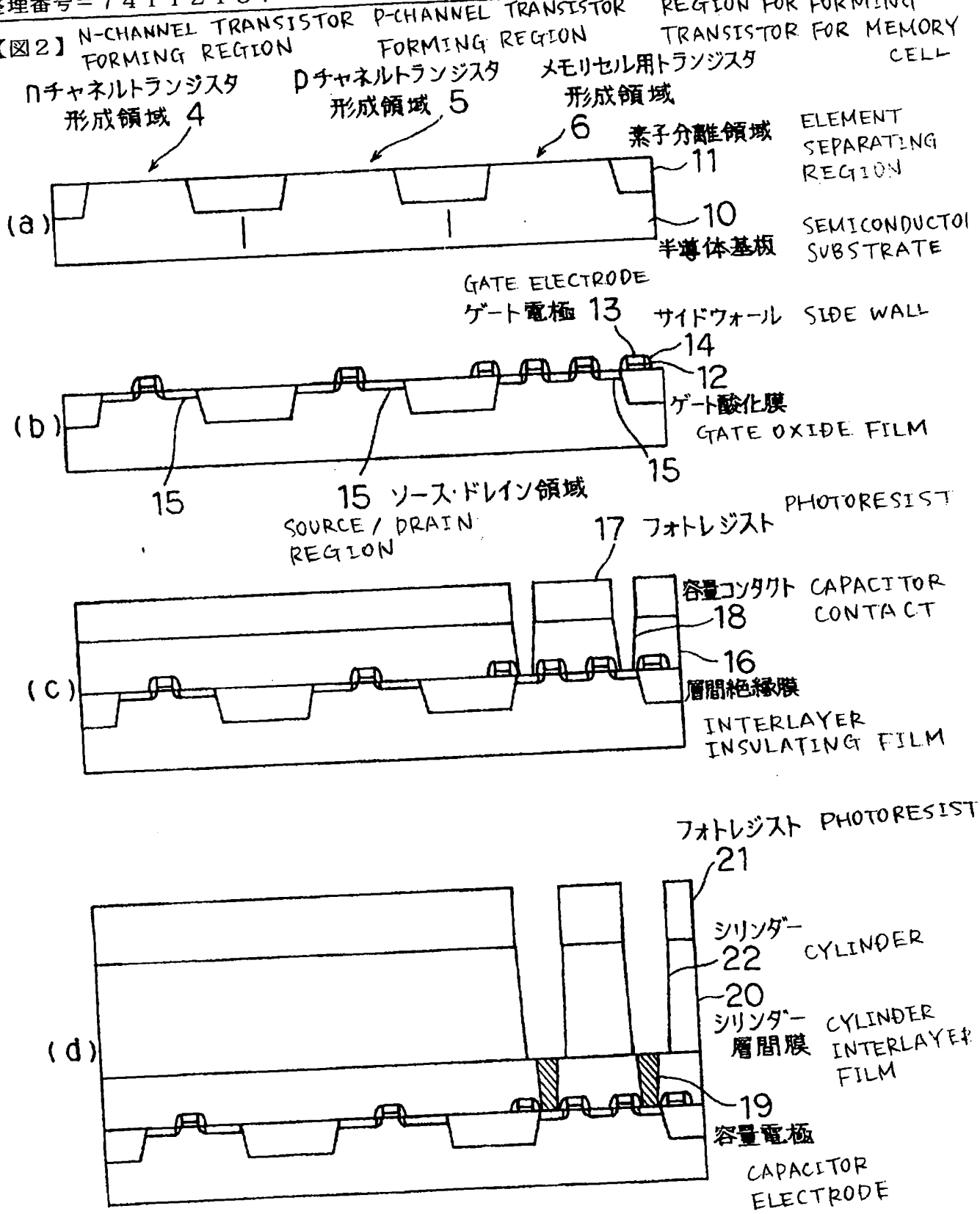
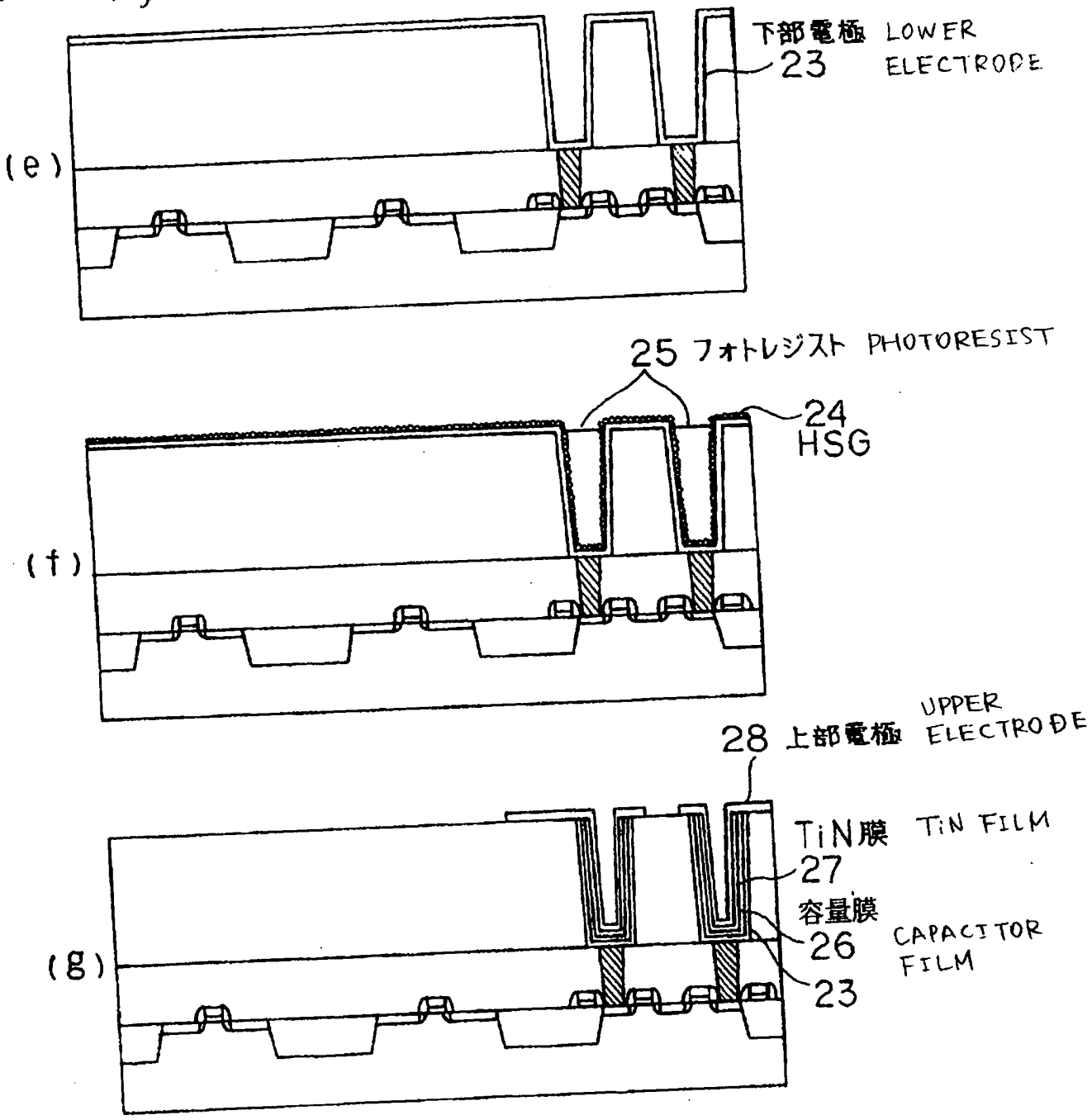


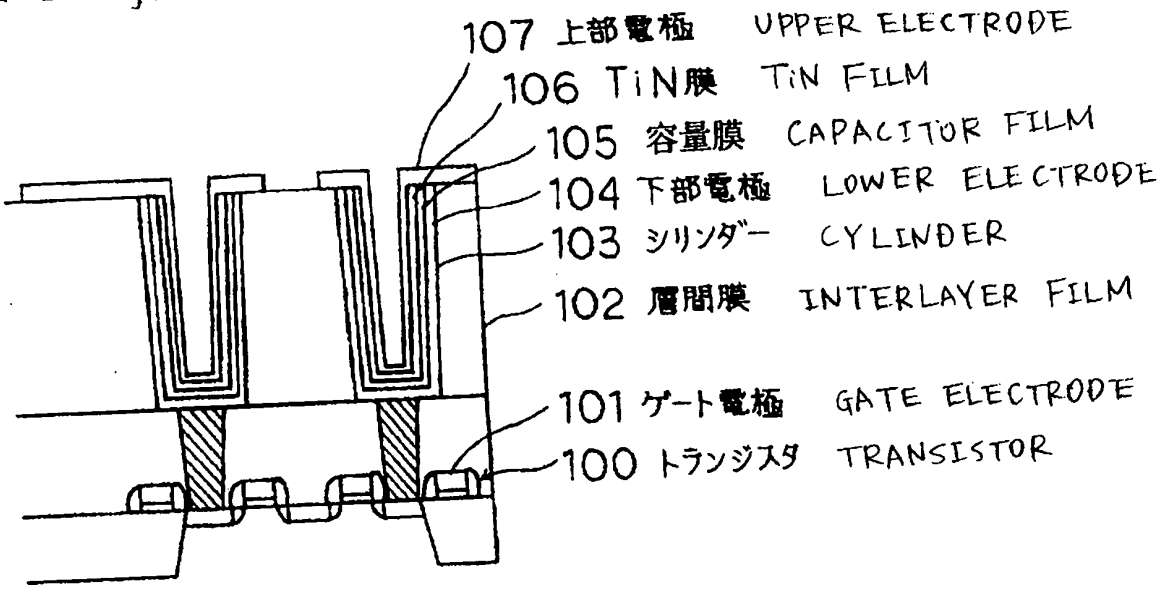
Fig.2【図２】


N-CHANNEL TRANSISTOR FORMING REGION
nチャネルトランジスタ形成領域 4
P-CHANNEL TRANSISTOR FORMING REGION
Pチャネルトランジスタ形成領域 5
REGION FOR FORMING TRANSISTOR FOR MEMORY CELL
メモリセル用トランジスタ形成領域 6
素子分離領域 ELEMENT SEPARATING REGION 11
(a)
10 半導体基板 SEMICONDUCTOR SUBSTRATE
GATE ELECTRODE ゲート電極 13
サイドウォール SIDE WALL 14
12 ゲート酸化膜 GATE OXIDE FILM
(b)
15
15 ソース・ドレイン領域 SOURCE / DRAIN REGION
17 フォトレジスト PHOTORESIST
容量コンタクト CAPACITOR CONTACT 18
16 層間絶縁膜 INTERLAYER INSULATING FILM
(c)
フォトレジスト PHOTORESIST 21
シリンダー CYLINDER 22
20 シリンダー層間膜 CYLINDER INTERLAYER FILM
19 容量電極 CAPACITOR ELECTRODE
(d)

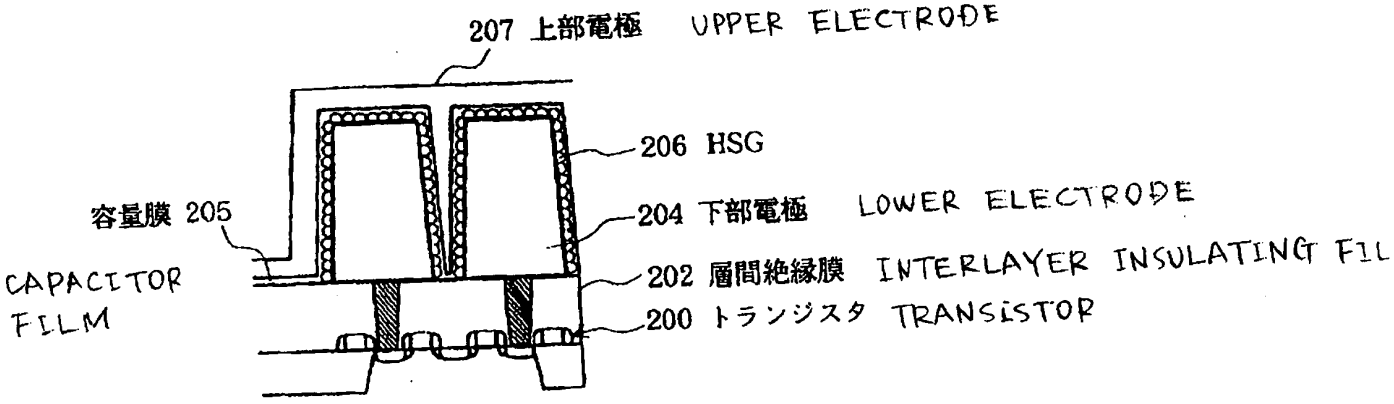
【図３】　Fig. 3


(e)
下部電極 LOWER ELECTRODE
23
(f)
25 フォトレジスト PHOTORESIST
24
HSG
(g)
28 上部電極 UPPER ELECTRODE
TiN膜 TiN FILM
27
容量膜
26 CAPACITOR FILM
23

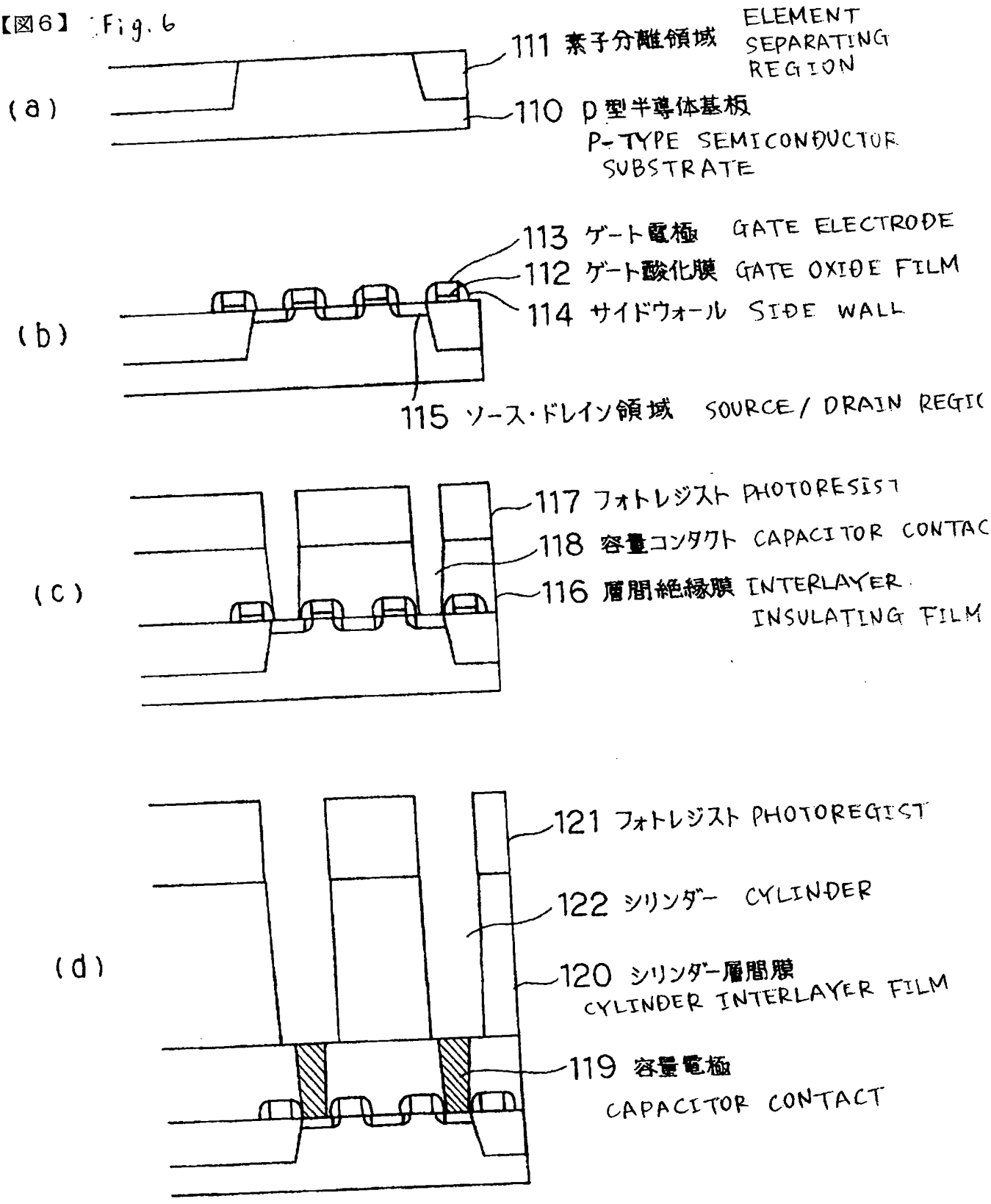
【図４】 Fig. 4



【図５】 Fig. 5

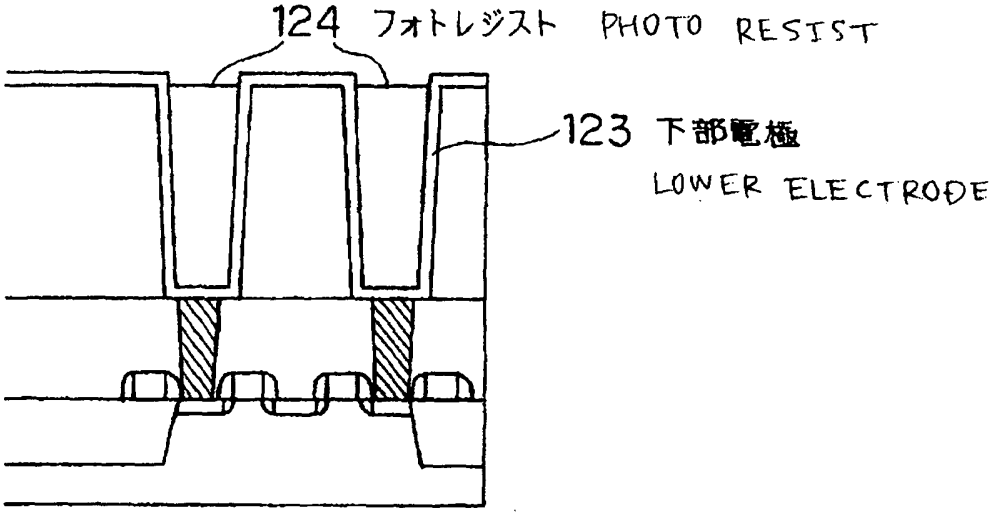


【図6】 Fig. 6

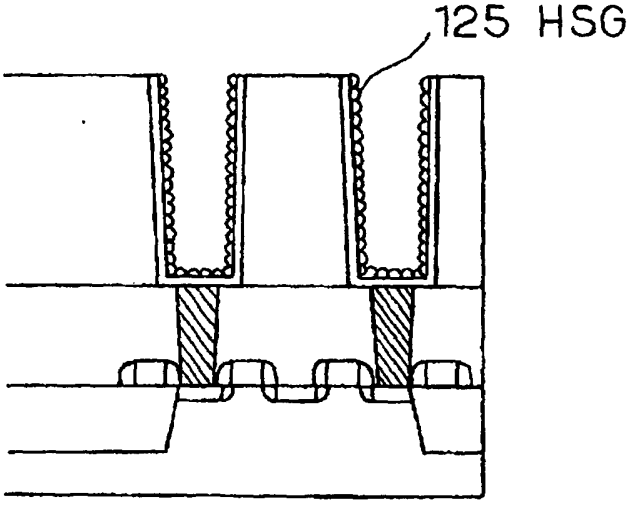

(a)
111 素子分離領域 ELEMENT SEPARATING REGION
110 P型半導体基板 P-TYPE SEMICONDUCTOR SUBSTRATE
(b)
113 ゲート電極 GATE ELECTRODE
112 ゲート酸化膜 GATE OXIDE FILM
114 サイドウォール SIDE WALL
115 ソース・ドレイン領域 SOURCE/DRAIN REGIO
(c)
117 フォトレジスト PHOTORESIST
118 容量コンタクト CAPACITOR CONTAC
116 層間絶縁膜 INTERLAYER INSULATING FILM
(d)
121 フォトレジスト PHOTOREGIST
122 シリンダー CYLINDER
120 シリンダー層間膜 CYLINDER INTERLAYER FILM
119 容量電極 CAPACITOR CONTACT

【図7】 Fig. 7

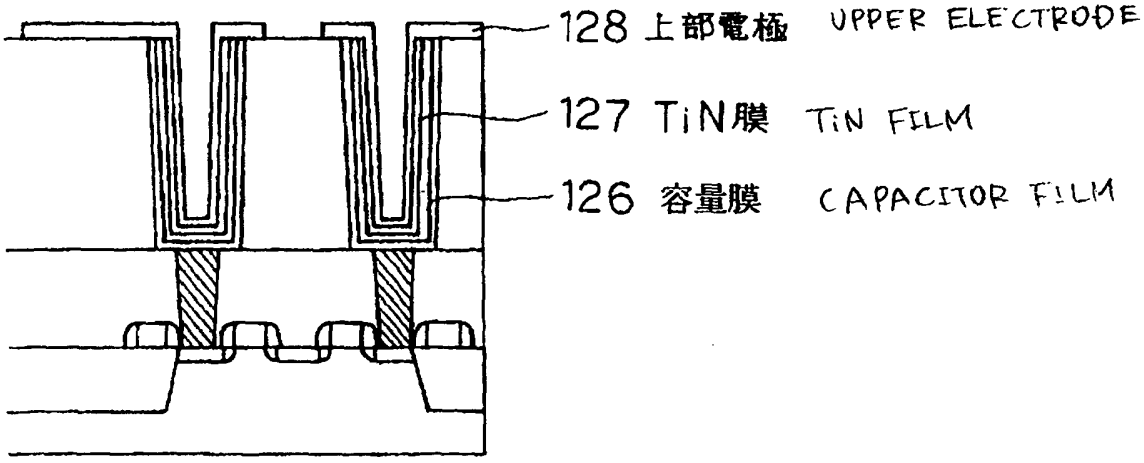
(e)


124 フォトレジスト PHOTO RESIST
123 下部電極
LOWER ELECTRODE

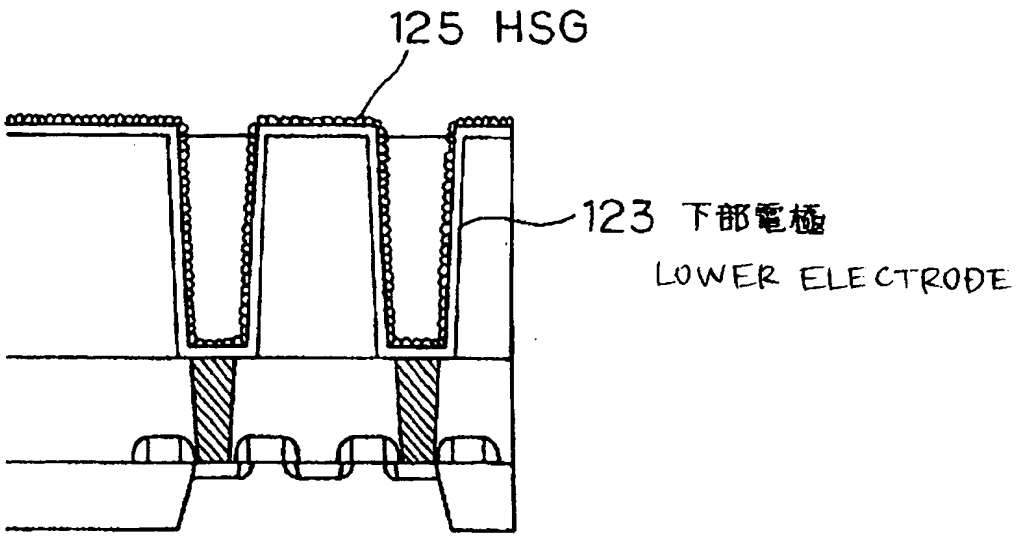
(f)


125 HSG

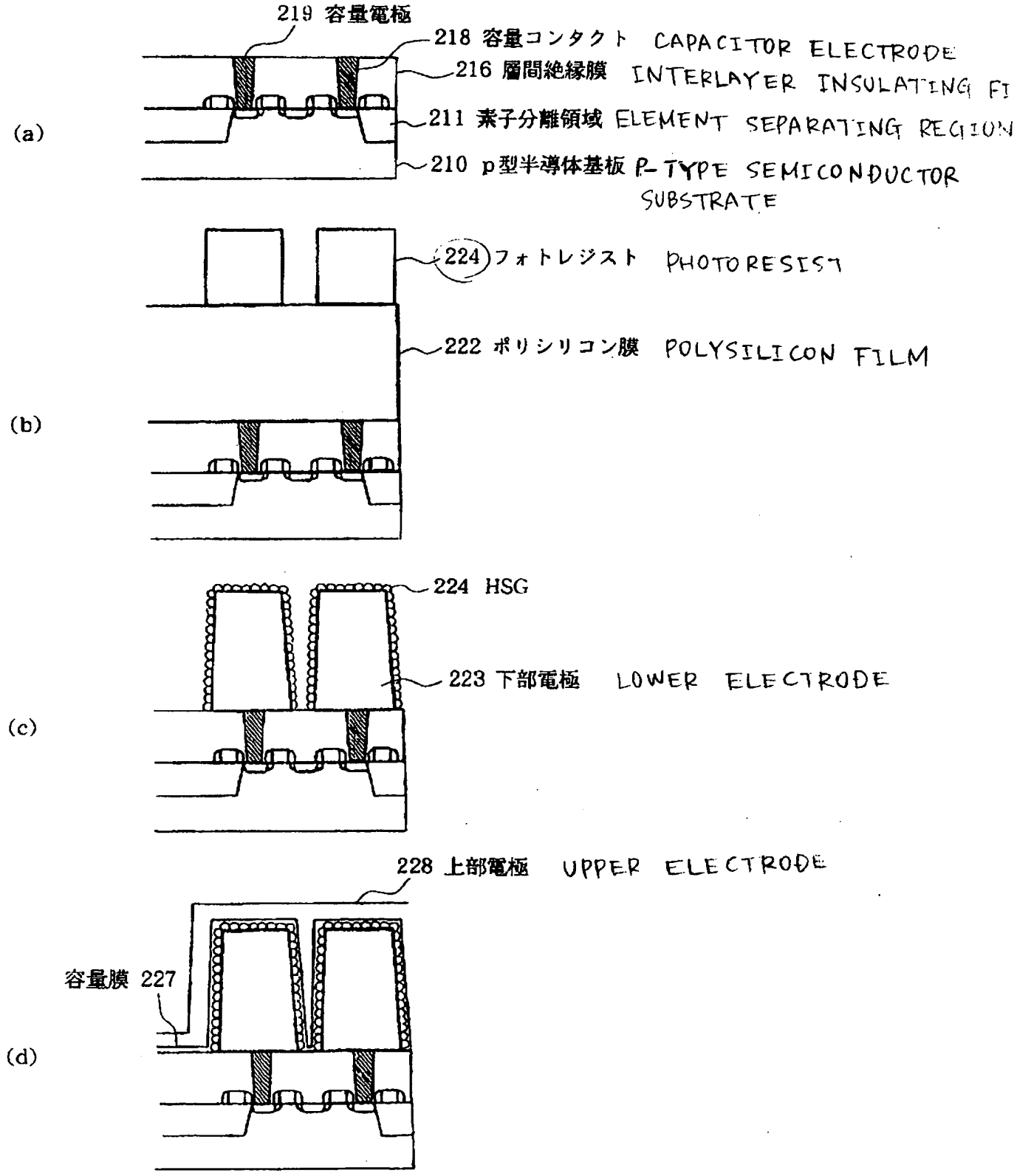
(g)


128 上部電極 UPPER ELECTRODE
127 TiN膜 TiN FILM
126 容量膜 CAPACITOR FILM

【図８】 Fig. 8



【図９】 Fig. 9


(a)
219 容量電極
218 容量コンタクト CAPACITOR ELECTRODE
216 層間絶縁膜 INTERLAYER INSULATING FI
211 素子分離領域 ELEMENT SEPARATING REGION
210 p型半導体基板 P-TYPE SEMICONDUCTOR SUBSTRATE
(b)
224 フォトレジスト PHOTORESIST
222 ポリシリコン膜 POLYSILICON FILM
(c)
224 HSG
223 下部電極 LOWER ELECTRODE
(d)
228 上部電極 UPPER ELECTRODE
容量膜 227

[Name of Document] Abstract

[Abstract]

[Problem] To provide a method of manufacturing a semiconductor device where HSG can be formed without fail on lower electrodes in cylinders for capacitor elements even when the semiconductor device has a CMOS logic circuit portion and a DRAM portion provided with a capacitor element of the cylinder structure mixedly mounted thereon.

[Solving Means] With regard to a method of manufacturing a semiconductor device with HSG formed on its lower electrode and with a DRAM having capacitor elements for storing information by accumulating signal charge and a logic device forming a logic circuit mixedly mounted thereon, a polysilicon film to be the lower electrode is formed on the inner wall of a cylinder as a groove provided in an interlayer film for forming the capacitor element and on the interlayer film, respectively, the HSG is formed on a polysilicon film formed in the cylinder and on the interlayer film, respectively, and the polysilicon film and the HSG on the interlayer film are removed with the polysilicon film and the HSG in the cylinder being left.

[Selected Drawing] Fig. 3